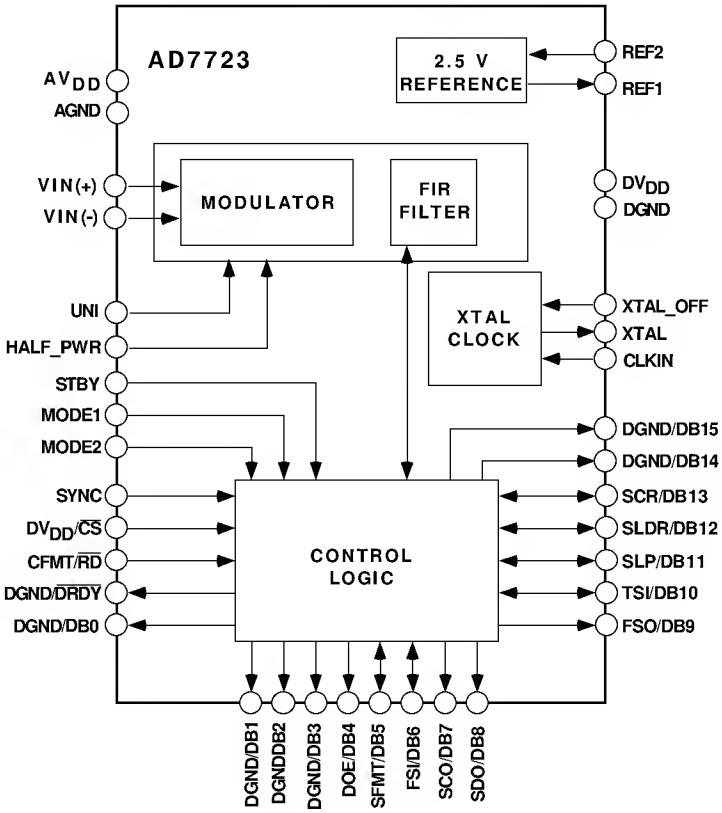
16-Bit, 1.2 MSPS CMOS, Sigma-Delta ADC

PRELIMINARY TECHNICAL DATA — AD7723

FEATURES

- 16-Bit Sigma-Delta ADC
  - 1.2 MSPS Output Word Rate
  - 32/16 X Oversampling Ratio
  - Low-Pass and Band-Pass Digital Filter
  - Linear Phase
- On-Chip 2.5 V Voltage Reference
- Standby Mode
- Flexible Parallel or Serial Interface
- Crystal Oscillator
- True Bipolar Input Operation
- Single +5 V Supply

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7723 is a complete 16-bit, sigma-delta ADC. The part operates from a +5 V supply. The analog input is continuously sampled, eliminating the need for an external sample-and-hold. The modulator output is processed by a finite impulse response (FIR) digital filter. The on-chip filtering combined with a high over-sampling-ratio reduces the external anti-alias requirements to first order in most cases. The digital filter frequency response can be programmed to be either low-pass or band-pass.

The AD7723 provides 16-bit performance for input bandwidths up to 460 kHz at an output word rate up to 1.2 MHz. The sample rate, filter corner frequencies and output word rate are set by the crystal oscillator or external clock frequency.

Data can be read from the device in either serial or parallel format. A stereo mode allows data from two devices to share a single serial data line. All interface modes offer easy, high-speed connections to modern digital signal processors.

The part provides an on-chip 2.5 V reference. Alternatively an external reference can be used.

A power down mode reduces the idle power consumption to 50 μW.

The AD7723 is available in a 44-pin PQFP package and is specified over the industrial temperature range from -40°C to +85°C.

Prelim. D, February 97

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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AD7723–SPECIFICATIONS[1] (AV_{DD} = +5V ± 5%; AGND = AGND1= DGND = 0V; F_{CLKIN} = 19.2 MHz; REF2 = 2.5 V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted)

Parameter	Test Conditions/Comments	B Version Min	Typ	Max	Units
DYNAMIC SPECIFICATIONS[2]					
Decimate by 32					
Signal to (Noise +Distortion)[3]		87			dB
Signal toNoise		90			dB
Total Harmonic Distortion[3]				-90	dB
Spurious Free Dynamic Range[3]		90			dB
Intermodulation Distortion		TBD			dB
Decimate by 16					
Signal to (Noise +Distortion)[3]	Measurement Bandwidth = 0.383*F_O	85			dB
Signal to (Noise +Distortion)[3]		81			dB
Signal toNoise		81			dB
Total Harmonic Distortion[3]				-90	dB
Spurious Free Dynamic Range[3]		90			dB
Intermodulation Distortion		TBD			dB
DIGITAL FILTER RESPONSE					
Low-Pass Decimate by 32					
0 kHz to F_{CLKIN}/83.5				± 0.001	dB
F_{CLKIN}/66.9		-3			dB
F_{CLKIN}/64		-6			dB
F_{CLKIN}/51.9 to F_{CLKIN}/2				-90	dB
Group Delay			1394/F_{CLKIN}		
Settling Time			2 *1394/F_{CLKIN}		
Low-Pass Decimate by 16					
0 kHz to F_{CLKIN}/41.75				± 0.001	dB
F_{CLKIN}/33.45		-3			dB
F_{CLKIN}/32		-6			dB
F_{CLKIN}/25.95 to F_{CLKIN}/2				-90	dB
Group Delay			594/F_{CLKIN}		
Settling Time			2 *594/F_{CLKIN}		
Band-Pass Decimate by 32					
F_{CLKIN}/51.90 to F_{CLKIN}/41.75				± 0.001	dB
F_{CLKIN}/62.95, F_{CLKIN}/33.34		-3			dB
F_{CLKIN}/64, F_{CLKIN}/32		-6			dB
0 kHz to F_{CLKIN}/83.5, F_{CLKIN}/25.95 to F_{CLKIN}/2				-90	dB
Group Delay			1394/F_{CLKIN}		
Settling Time			2 *1394/F_{CLKIN}		
Output Data Rate, F_O					
Decimate by 32			F_{CLKIN}/32		
Decimate by 16			F_{CLKIN}/16		
ANALOG INPUTS					
Full Scale Input Span	VIN(+) - VIN(-)				
Bipolar Mode				±4/5*V_{REF2}	V
Unipolar Mode		0		8/5*V_{REF2}	V
Absolute Input Voltage	VIN (+) and/or VIN (-)	AVSS		AVDD	V
Input Sampling Capacitance			2		pF
Input Sampling Rate,F_{CLKIN}				19.2	MHz
CLOCK					
CLKIN Duty Ratio		45		55	%

NOTES

[1]Operating Temperature Range is as follows :B Version ; -40°C to +85°C

[2]Measurement Bandwidth = 0.5*F_OInput Level = -0.05dB

[3]For preproduction samples, these specification apply with use of an external reference. When using the internal reference THD will degrade to about -84 dB unless a large capacitor is used to bypass the REF2 pin. A 10µF tantalum capacitor from REF2 to AGND2 gives good distortion performance down to 10 kHz input signals.

Specifications subject to change without notice.

AD7723–SPECIFICATIONS[1] (AV_{DD} = +5V ± 5%; AGND = AGND1= DGND = 0V; F_{CLKIN} = 19.2 MHz; REF2 = 2.5 V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted)

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
REFERENCE					
REF1 Output Resistance			3		kΩ
Reference Buffer					
Offset Voltage	Offset between REF1 and REF2		± 10		mV
Using Internal Reference					
REF2 Output Voltage		2.39	2.5	2.61	V
REF2 Output Voltage Drift			60		ppm/°C
Using External Reference					
REF2 Input Impedance	REF1 = AGND				kΩ
REF2 External Voltage Range		1.2	2.5	3.15	V
STATIC PERFORMANCE					
Resolution		16			Bits
DC CMRR		80			dB
Offset Error					
Bipolar Mode			±5		mV
Unipolar Mode			±25		mV
Gain Error[3,4]			± 0.5		%FSR
LOGIC INPUTS (Excluding CLKIN)					
V_{INH}, Input High Voltage		2.0			V
V_{INL}, Input Low Voltage				0.8	V
CLOCK INPUT (CLKIN)					
V_{INH}, Input High Voltage		3.8			V
V_{INL}, Input Low Voltage				0.4	V
ALL LOGIC INPUTS					
I_{IN}, Input Current	V_{IN} = 0 V to DV_{DD}			± 10	µA
C_{IN}, Input Capacitance				10	pF
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	$\|I_{OUT}\|$ = 200 µA	4.0			V
V_{OL}, Output Low Voltage	$\|I_{OUT}\|$ = 1.6 mA			0.4	V
POWER SUPPLIES					
AV_{DD}		4.75		5.25	V
I_{AVDD}	HALF_PWR = Logic Low				mA
	HALF_PWR = Logic High				mA
DV_{DD}		4.75		5.25	V
I_{DVDD}					mA
Power Consumption	Active Mode				mW
Power Consumption	Standby Mode			50	µW

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C Unless Otherwise Noted)

DV_{DD} to DGND ..... -0.3 V to 7 V
AV_{DD}, AV_{DD1} to AGND ..... -0.3 V to 7 V
AV_{DD}, AV_{DD1} to DV_{DD} ..... -1 V to +1 V
AGND, AGND1 to DGND ..... -0.3 V to +0.3 V
Digital Inputs to DGND ..... -0.3 V to DV_{DD} + 0.3 V
Digital Outputs to DGND ..... -0.3 V to DV_{DD} + 0.3 V
VIN(+), VIN(-) toAGND ..... -0.3 V to AV_{DD} + 0.3V
REF1 to AGND ..... -0.3 V to AV_{DD} + 0.3V
REF2 to AGND ..... -0.3 V to AV_{DD} + 0.3V
DGND, AGND ..... ±0.3 V
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
θ_{JA} Thermal Impedance ..... 95°C/W
Lead Temperature, Soldering
Vapor Phase(60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

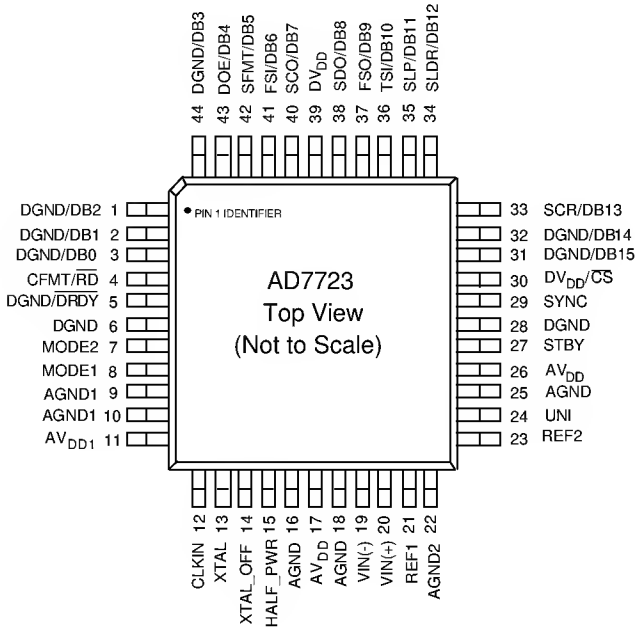
NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7723 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
44-PIN PQFP PACKAGE



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7723BS	-40°C to +85°C	S-44

* S = 44-Pin, PQFP Package

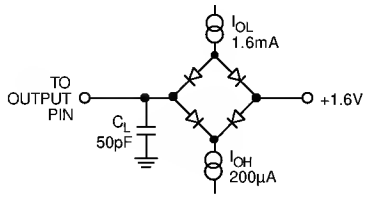


Figure 1. Load Circuit for Timing Specifications

TIMING SPECIFICATIONS (AV_{DD} = +5V ± 5%; AGND = AGND1= DGND = 0V; F_{CLKIN} = 19.2 MHz; C_L = 50 pF; SFMT = Logic Low or High, CFMT = Logic Low or High; T_A = T_{MIN} to T_{MAX}; unless otherwise noted)

	Symbol	Min	Typ	Max	Units
CLKIN Frequency	F_{CLK}	1		19.2	MHz
CLKIN Period (t_{CLK} = 1/F_{CLK})	t_1	0.052		1	µs
CLKIN Low Pulse Width	t_2	0.45 *t_1		0.55 *t_1	
CLKIN High Pulse Width	t_3	0.45 *t_1		0.55 *t_1	
CLKIN Rise Time	t_4	5			ns
CLKIN Fall Time	t_5	5			ns
FSI Low Time	t_6	2			t_{CLK}
FSI Setup Time	t_7	20			ns
FSI Hold Time	t_8	20			ns
CLKIN to SCO Delay	t_9		40		ns
SCO Period[1], SCR = 1	t_{10}		2		t_{CLK}
SCO Period[1], SCR = 0	t_{10}		1		t_{CLK}
SCO transition to FSO High Delay	t_{11}		2	5	ns
SCO transition to FSO Low Delay	t_{12}		2	5	ns
SCO transition to SDO Valid Delay	t_{13}		3	8	ns
SCO transition from FSI[2]	t_{14}			t_{CLK}+t_2	
SDO Enable Delay Time	t_{15}		30	45	ns
SDO Disable Delay Time	t_{16}		10	30	ns
$\overline{DRDY}$ High Time[1]	t_{17}	2			t_{CLK}
Conversion Time[1] (Refer to Table I and II)	t_{18}	16/32			t_{CLK}
$\overline{DRDY}$ to $\overline{CS}$ Setup Time	t_{19}	0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{20}	0			ns
$\overline{RD}$ Pulse Width	t_{21}	t_{CLK} + 20			ns
Data Access Time after $\overline{RD}$ Falling Edge[3]	t_{22}			t_{CLK} + 40	ns
Bus Relinquish Time after $\overline{RD}$ Rising Edge	t_{23}			t_{CLK} + 40	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{24}	0			ns
$\overline{RD}$ to $\overline{DRDY}$ High Time	t_{25}			1	t_{CLK}
SYNC Input Pulse Width	t_{26}	10			ns
$\overline{SYNC}$ Low Time Before CLKIN Rising	t_{27}	10			ns
$\overline{DRDY}$ High Delay after $\overline{SYNC}$ Low	t_{28}			50	ns
$\overline{DRDY}$ Low Delay after $\overline{SYNC}$ Low	t_{29}				t_{CLK}

NOTES
1 Guaranteed by design.
2 Frame Sync is initiated on the falling edge of CLKIN.
3 With RD synchronous to CLKIN, t_{22} can be reduced up to 1 t_{clk}

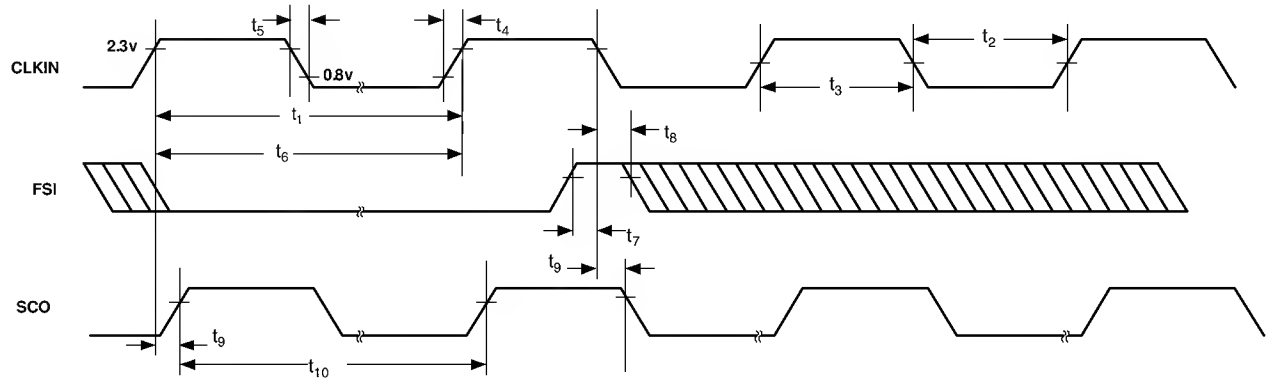


Figure 2. Serial Mode Timing for Clock Input, Frame Sync Input, and Serial Clock Output

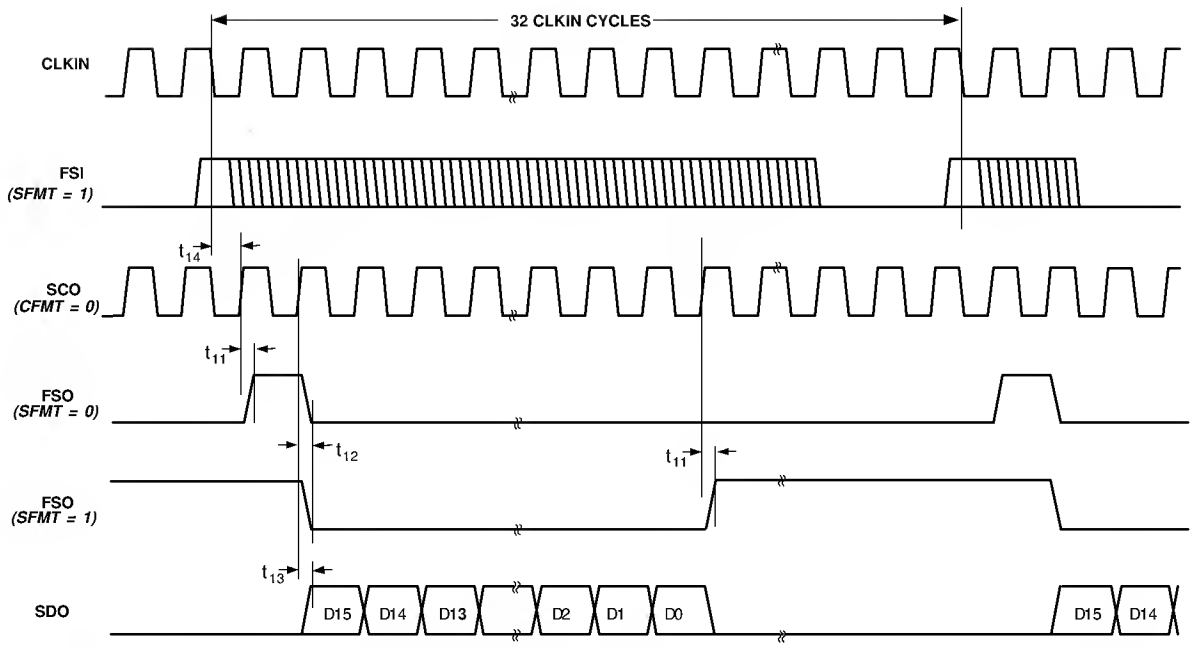


Figure 3. Serial Mode 1. Timing for Frame Sync Input, Frame Sync Output, Serial Clock Output, and Serial Data Output (Refer to Table I. for Control Inputs, TSI = DOE)

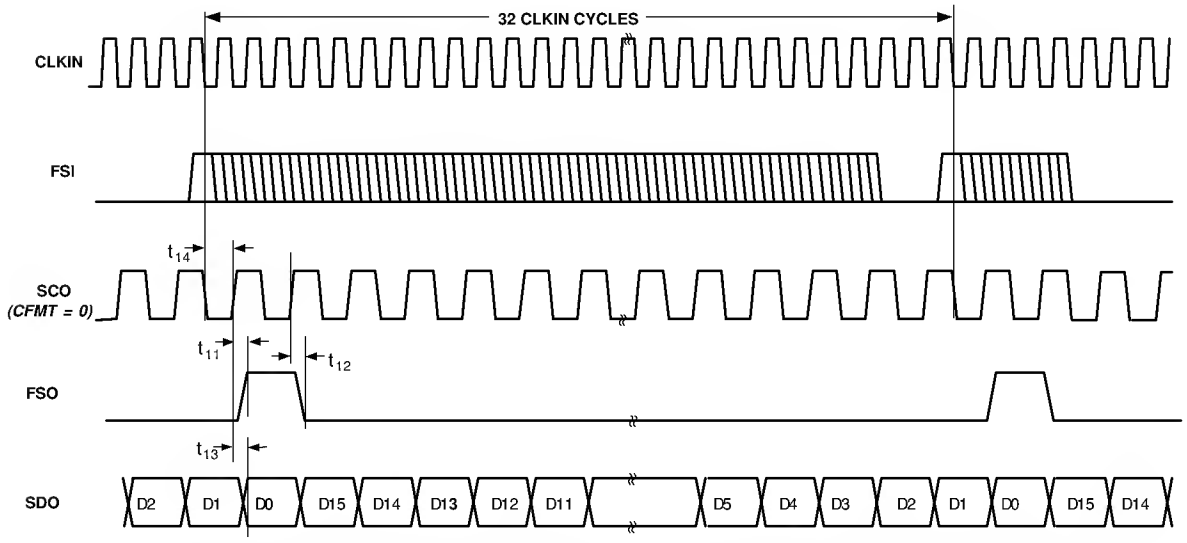


Figure 4. Serial Mode 2. Timing for Frame Sync Input, Frame Sync Output, Serial Clock Output, and Serial Data Output (Refer to Table I. for Control Inputs, TSI = DOE)

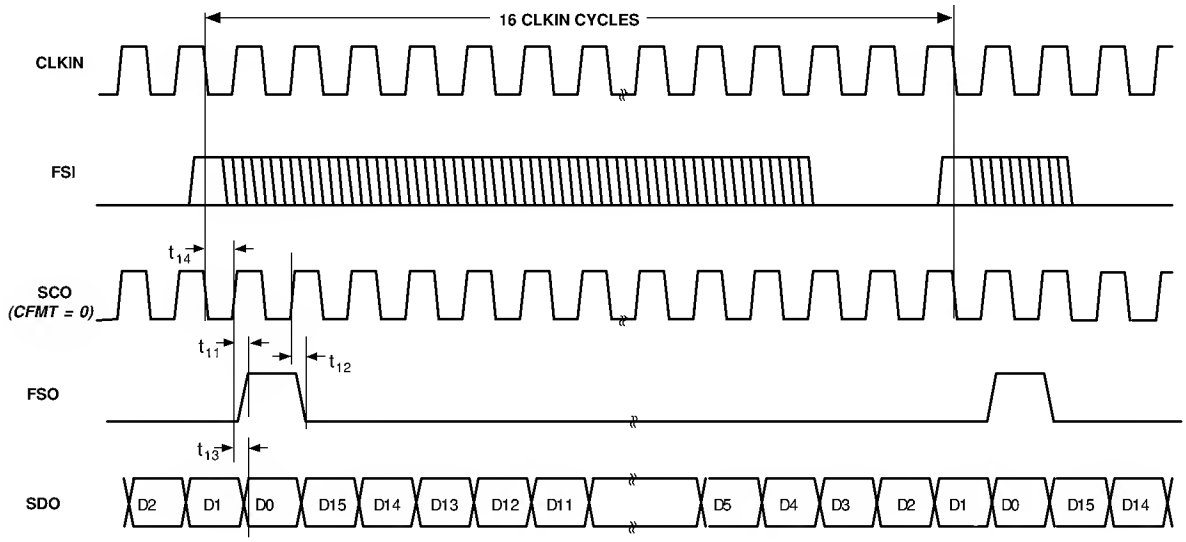


Figure 5. Serial Mode 3. Timing for Frame Sync Input, Frame Sync Output, Serial Clock Output, and Serial Data Output (Refer to Table I. for Control Inputs, TSI = DOE)

TABLE I. SERIAL INTERFACE (MODE1 = 0, MODE2 = 0)

Serial Mode	Decimation Ratio (SLDR)	Digital Filter Mode (SLP)	SCO Frequency (SCR)	Output Data Rate	Control Inputs SLDR	SLP	SCR
1	32	Low-Pass	F_{CLKIN}	F_{CLKIN} /32	1	1	0
1	32	Band-Pass	F_{CLKIN}	F_{CLKIN} /32	1	0	0
2	32	Low-Pass	F_{CLKIN} /2	F_{CLKIN} /32	1	1	1
2	32	Band-Pass	F_{CLKIN} /2	F_{CLKIN} /32	1	0	1
3	16	Low-Pass	F_{CLKIN}	F_{CLKIN} /16	0	1	0

TABLE II. PARALLEL INTERFACE

Digital Filter Mode	Decimation Ratio	Output Data Rate	Control Inputs MODE1	MODE2
Band-Pass	32	F_{CLKIN} /32	0	1
Low-Pass	32	F_{CLKIN} /32	1	0
Low-Pass	16	F_{CLKIN} /16	1	1

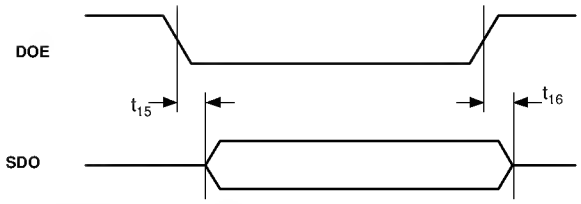


Figure 6. Serial Mode Timing for Data Output Enable and Serial Data Output

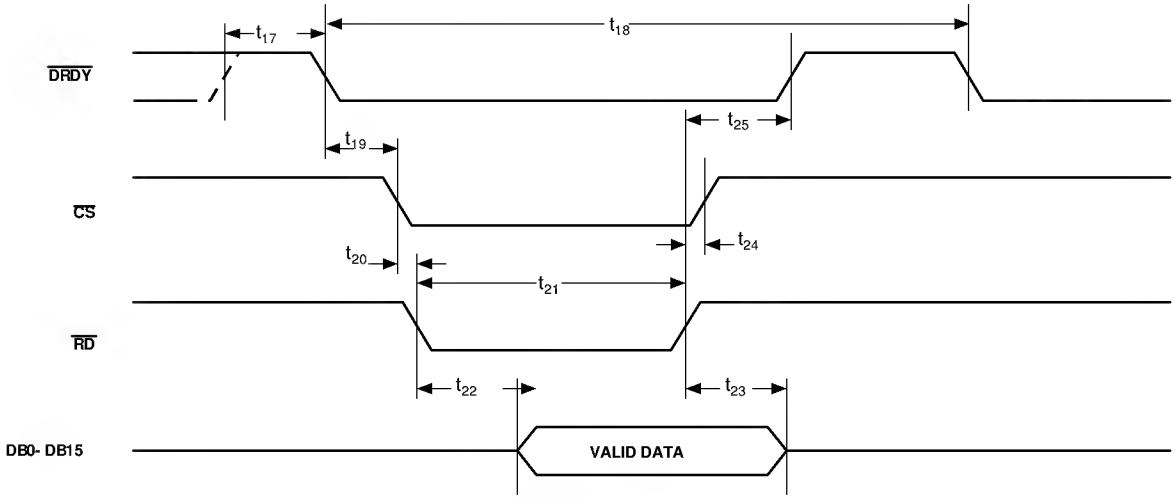


Figure 7. Parallel Mode Read Timing

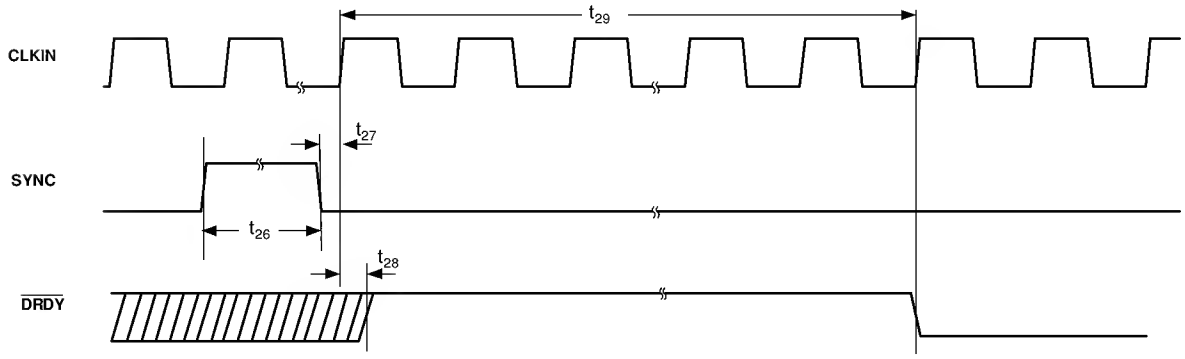


Figure 8. SYNC and RESET Timing Serial and Parallel Mode

PIN FUNCTION DESCRIPTION

Mnemonic	Pin No.	Description
AV_{DD1}	11	Digital logic power supply voltage for the analog modulator.
AGND1	9,10	Digital logic power supply ground for the analog modulator.
AV_{DD}	17, 26	Positive power supply voltage for the analog modulator.
AGND	16, 18, 25	Power supply ground for the analog modulator.
AGND2	22	Power supply ground returnto the reference circuitry, REF2, of the analog modulator.
DV_{DD}	39	Digital Power Supply Voltage; +5 V±5%
DGND	6, 28	Ground reference for digital circuitry.
REF1	21	Reference Output. REF1 connects through 3 kΩ to the output of the internal 2.5 V reference and to a buffer amplifier that drives the Σ-Δ modulator.
REF2	23	Reference Input. REF2 connects to the output of an internal buffer amplifier that drives the Σ-Δ modulator. When REF2 is used as an input, REF1 must be connected to AGND to disable the internal buffer amplifier.
VIN(+)	20	Positive terminal of the differential analog input.
VIN(-)	19	Negative terminal of the differential analog input.
UNI	24	Analog input range select input. The UNI pin selects the analog input range for either bipolar or unipolar operation. A logic high input selects unipolar operation and a logic low selects bipolar operation.
CLKIN	12	Clock input. An external clock source can be applied directly to this pin with XTAL_OFF tied high. Alternatively, a parallel resonant fundamental frequency crystal, in parallel with a 1 MΩ resistor can be connected between the XTAL pin and the CLKIN pin with XTAL_OFF tied low. External capacitors are then required from the CLKIN and XTAL pins to ground. Consult the crystal manufacturer's recommendation for the load capacitors.
XTAL	13	Input to crystal oscillator amplifier. If an external clock is used, XTAL should be tied to AV_{SS}.
XTAL_OFF	14	Oscillator enable input. A logic high disables the crystal oscillator amplifier to allow use of an external clock source. Set low when using an external crystal between the CLKIN and XTAL pins.
MODE1/2	8, 7	Mode control inputs. The MODE1 and MODE2 pins choose either parallel or serial data interface operation and select the operating mode for the digital filter in parallel mode. Refer to Table I and II.
HALF_PWR	15	When set high, the power dissipation is reduced by approximately one-half and a maximum CLKIN frequency of 10 MHz applies.
SYNC	29	Synchronization logic input. When using more than one AD7723, operated from a common master clock, SYNC allows each ADC to simultaneously sample its analog input and update its output register. A rising edge resets the AD7723 digital filter sequencer counter to zero. When the rising edge of CLKIN senses a logic low on SYNC the reset state is released.
STBY	27	Standby logic input. A logic high sets the AD7723 into the power-down state.

PARALLEL MODE PIN FUNCTION DESCRIPTION

Mnemonic	Pin No.	Description
$DV_{DD}/\overline{CS}$	30	Chip select logic input.
CFMT/$\overline{RD}$	4	Read logic input. Used in conjunction with $\overline{CS}$ to read data from the parallel bus. The output data bus is enabled when the rising edge of CLKIN senses a logic low level on $\overline{RD}$ if $\overline{CS}$ is also low. When $\overline{RD}$ is sensed high, the output data bits, DB15-DB0 will be high impedance.
DGND/$\overline{DRDY}$	5	Data ready logic output. A falling edge indicates a new output word is available to be read from output data register. DRDY will return high upon completion of a read operation. If a read operation does not occur between output updates, DRDY will pulse high for two CLKIN cycles before the next output update. DRDY also indicates when conversion results are available after a SYNC sequence.
DGND/DB15	31	Data output bit, (MSB)
DGND/DB14	32	Data output bit
SCR/DB13	33	Data output bit
SLDR/DB12	34	Data output bit
SLP/DB11	35	Data output bit
TSI/DB10	36	Data output bit
FSO/DB9	37	Data output bit
SDO/DB8	38	Data output bit
SCO/DB7	40	Data output bit
FSI/DB6	41	Data output bit
SFMT/DB5	42	Data output bit
DOE/DB4	43	Data output bit
DGND/DB3	44	Data output bit
DGND/DB2	1	Data output bit
DGND/DB1	2	Data output bit
DGND/DB0	3	Data output bit, (LSB)

SERIAL MODE PIN FUNCTION DESCRIPTION

Mnemonic	Pin No.	Description
CFMT/$\overline{RD}$	4	Serial clock format logic input. The clock format pin selects whether the serial data, SDO, is valid on the rising or falling edge of the serial clock, SCO. When CFMT is logic low, serial data is valid on the falling edge of the serial clock, SCO. If CFMT is logic high, SDO is valid on the rising edge of SCO .
DOE/DB4	43	Data output enable Logic Input. The DOE pin controls the three-state output buffer of the SDO pin. The active state of DOE is determined by the logic level on the TSI pin. When the DOE logic level equals the level on TSI pin the serial data output, SDO, is active. Otherwise SDO will be high impedance. SDO can be three-state after a serial data transmission by connecting DOE to FSO.
SFMT/DB5	42	Serial data format logic input. The logic level on the SFMT pin selects the format of the FSO signal. A logic low makes the FSO output a pulse, one SCO cycle wide. With SFMT set to a logic high the FSO signal is a frame pulse which is active low for the duration of the 16 data bit transmission.
FSI/DB6	41	Frame sychronization logic input. The FSI input is used to synchronize the AD7723 serial output data register to an external source. When the falling edge of CLKIN detects a low to high transition, the AD7723 interrupts the current data transmission, reloads the output serial shift register, resets SCO, and transmits the conversion result. Synchronization starts immediately and the next 32 conversions are invalid. FSI inputs applied at exact integer multiples of the output data rate do not alter the serial data transmission. If FSI is tied to either a logic high or low the AD7723 will generate FSO outputs, controlled by the logic level on SFMT.
SCO/DB7	40	Serial data clock output.
SDO/DB8	38	Serial data output. The serial data is shifted out MSB first, synchronous with the SCO. Serial Mode 1 data transmissions last 32 SCO cycles. After the LSB is output, trailing zeros are output for the remaining 16 SCO cycles. Serial Mode 2 and 3 data transmissions last 16 SCO cycles.
FSO/DB9	37	Frame sync output. This output indicates the beginning of a word transmission on the SDO pin. Depending on the logic level of the SFMT pin, the FSO signal is either a positive pulse approximately one SCO period wide, or a frame pulse which is active low for the duration of the 16 data bit transmission.
TSI/DB10	36	Time Slot Logic Input. The logic level on TSI sets the active state of the DOE pin. With TSI set logic high, DOE will enable the SDO output buffer when it is a logic high, and vice versa. TSI is used when two AD7723s are connected to the same data serial data bus.
SLP/DB11	35	Serial mode low-pass/band-pass filter select input. With SLP pin set logic high, the low-pass filter response is selected. A logic low selects band-pass.
SLDR/DB12	34	Serial mode low/high output data rate select input. With SLDR set logic high, the low data rate is selected. A logic low selects the high data rate. The high data rate corresponds to data at the output of the 4th decimation filter (Decimate by 16). The low data rate corresponds to data at the output of the 5th decimation filter (Decimate by 32).
SCR/DB13	33	Serial clock rate select input. With SCR set logic low, the serial clock output frequency, SCO, is equal to the CLKIN frequency. A logic high sets it equal to one-half the CLKIN frequency.
DV_{DD}/$\overline{CS}$	30	Tie to DV_{DD}
DGND/DB14	32	Tie to DGND.
DGND/DB15	31	Tie to DGND.
DGND/$\overline{DRDY}$	5	Tie to DGND.
DGND/DB0	3	Tie to DGND.
DGND/DB1	2	Tie to DGND.
DGND/DB2	1	Tie to DGND.
DGND/DB3	44	Tie to DGND.
DGND/DB14	32	Tie to DGND.
DGND/DB15	31	Tie to DGND.

TERMINOLOGY

Signal-to-Noise plus Distortion Ratio (S/(N+D))
S/(N+D) is the measured signal-to-noise plus distortion ratio at the output of the ADC. The signal is the RMS magnitude of the fundamental. Noise plus distortion is the rms sum of all of the nonfundamental signals and harmonics up to half the Output DataRate ($F_O/2$), excluding dc. The ADC is evaluated by applying a low noise, low distortion sine wave signal to the input pins. By generating a Fast Fourier Transform (FFT) plot, the S/(N+D) data can then be obtained from the output spectrum.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the harmonics to the rms value of the fundamental. THD is defined as:

$$THD = 20\log ((SQRT(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)) / V_1)$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics. The THD is also derived from the FFT plot of the ADC output spectrum.

Spurious Free Dynamic Range (SFDR)
Defined as the difference, in dB, between the peak spurious or harmonic component in the ADC output spectrum (up to $F_O/2$ and excluding dc) and the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the output spectrum of the FFT. For input signals whose second harmonics occur in the stop band region of the digital filter the spur in the noise floor limits the SFDR

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Testing is performed using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamental expressed in dB.

Pass-Band Ripple
The frequency response variation of the AD7723 in the defined pass-band frequency range.

Pass-Band Frequency
The frequency up to which the frequency response variation is within the pass-band ripple specification.

Cut-Off Frequency
The frequency below which the AD7723's frequency response will not have more than 3 dB of attenuation.

Stop-Band Frequency
The frequency above which the AD7723's frequency response will be within its stop-band attenuation.

Stop-Band Attenuation
The AD7723's frequency response will not have less than 90 dB of attenuation in the stated frequency band.

Integral Nonlinearity
This is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are minus full scale, a point 0.5 LSB below the first code transition (100 . . . 00 to 100 . . . 01 in bipolar mode, 000 . . . 00 to 000 . . . 01 in unipolar mode) and plus full scale, a point 0.5 LSB above the last code transition (011 . . . 10 to 011 . . . 11 in bipolar mode, 111 . . . 10 to 111 . . . 11 in unipolar mode). The error is expressed in LSBs.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between two adjacent codes in the ADC.

Common Mode Rejection Ratio
The ability of a device to reject the effect of a voltage applied to both input terminals simultaneously—often through variation of a ground level—is specified as a common-mode rejection ratio. CMRR is the ratio of gain for the differential signal to the gain for the common-mode signal.

Unipolar Offset Error
Unipolar offset error is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal differential voltage (VIN(+) - VIN(-)+ 0.5 LSB) when operating in the unipolar mode.

Bipolar Offset Error
This is the deviation of the midscale transition code (111 . . . 11 to 000 . . . 00) from the ideal differential voltage (VIN(+) - VIN(-) - 0.5 LSB) when operating in the bipolar mode.

Gain Error
The first code transition should occur at an analog value 1/2 LSB above –full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

CIRCUIT DESCRIPTION

The AD7723 ADC employs a sigma-delta conversion technique to convert the analog input into an equivalent digital word. The modulator samples the input waveform and outputs an equivalent digital word at the input clock frequency, F_{CLKIN}.

Due to the high oversampling rate, which spreads the quantization noise from 0 to Fsample/2, the noise energy contained in the band of interest is reduced (Figure 9a). To reduce the quantization noise further, a high order modulator is employed to shape the noise spectrum, so that most of the noise energy is shifted out of the band of interest (Figure 9b).

The digital filter that follows the modulator removes the large out of band quantization noise, (Figure 9c) while also reducing the data rate from Fsample at the input of the filter to Fsample/32 or Fsample/16 at the output of the filter, depending on the state on the MODE1/2 pins in parallel interface mode or the pin SLDR in serial interface mode. The AD7723 output data rate is a little over twice the signal bandwidth, which guarantees that there is no loss of data in the signal band.

Digital filtering has certain advantages over analog filtering. Firstly, since digital filtering occurs after the A/D conversion, it can remove noise injected during the conversion process. Analog filtering cannot remove noise injected during conversion. Secondly, the digital filter combines low passband ripple with a steep roll off, while also maintaining a linear phase response.

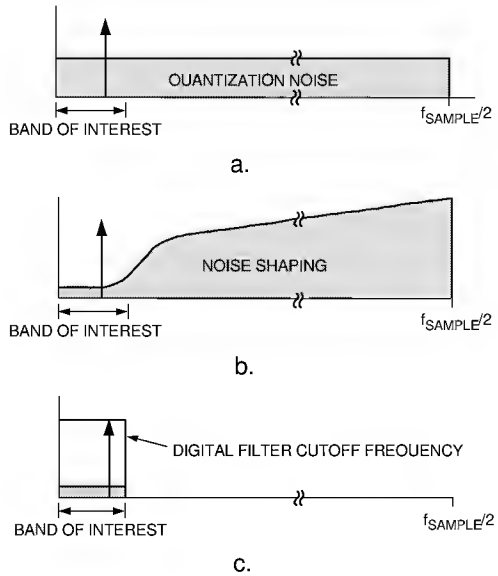


Figure 9. Sigma-Delta ADC

The AD7723 employs 4 or 5 Finite Impulse Response (FIR) filters in series. Each individual filter's output data rate is half that of the filter's input data rate. When data is fed to the interface from the output of the 4th filter the output data rate is Fsample/16 and the resulting Over Sampling Ratio (OSR) of the converter is 16. Data fed to the interface from the output of the 5th filter results in an output data rate of Fsample/32 and a corresponding OSR for the converter of 32. When an Output Data Rate of Fsample/32 is selected, the digital filter response can be set to either low-pass or band-pass. The band-pass response is useful when the input signal is band limited since the resulting output data rate is half that required to convert the band when the low pass operating mode is used. To illustrate the operation of this mode consider a band- limited signal as shown in Figure 10a. This signal band can be correctly converted by selecting the (low-pass) ODR=Fsample/16 mode, as shown in Figure 10b. Note that the output data rate is a little over twice the maximum frequency in the frequency band. Alternatively the band-pass mode can be selected as shown in Figure 10c. The band-pass filter removes unwanted signals from DC to just below Fsample/64. Rather than outputting data at Fsample/16 the output of the bandpass filter is sampled at Fsample/32. This affectively translates the wanted band to a maximum frequency of a little less than Fsample/64 as shown in Figure 10d. Halving the output data rate reduces the work load of any following signal processor and also allows a lower serial clock rate to be used.

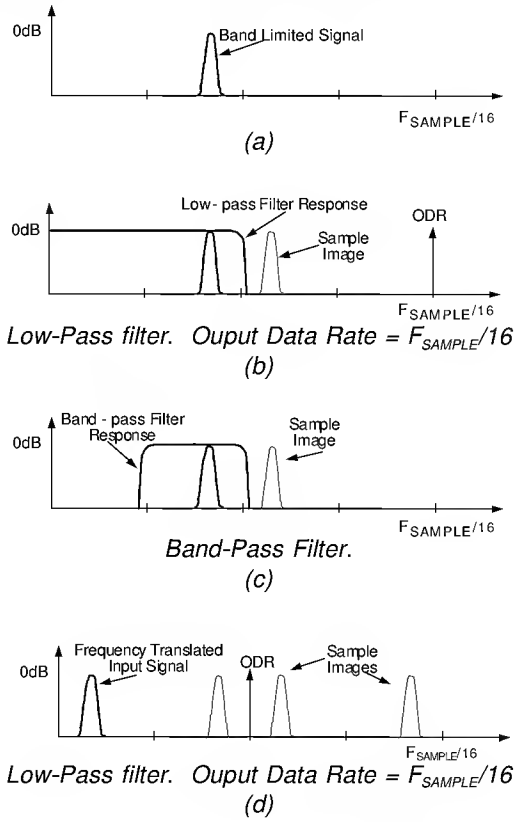


Figure 10. Band-pass Operation

The frequency response of the 3 digital filter operating modes is shown in Figure 11a, 11b, and 11c.

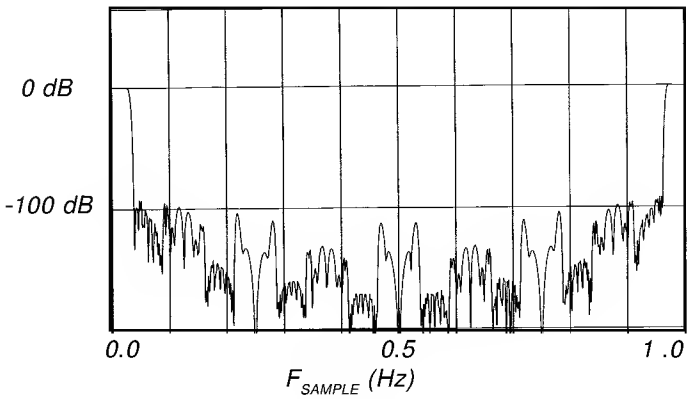


Figure 11a. Low-Pass Filter Decimate by 16

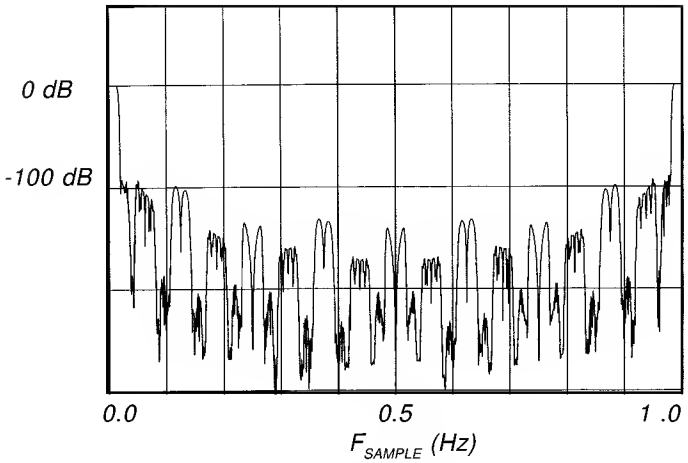


Figure 11b. Low-Pass Filter Decimate by 32

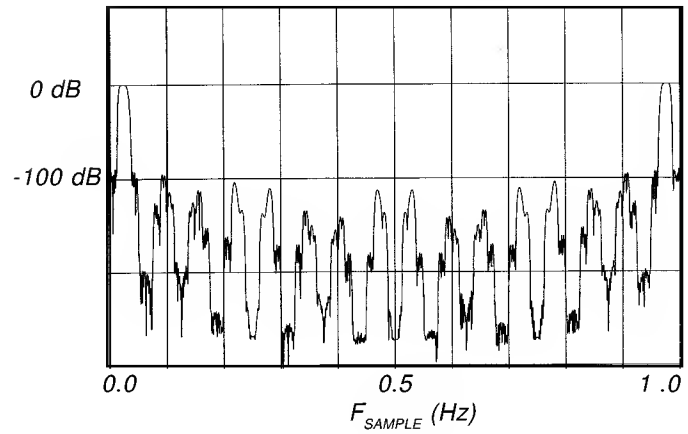


Figure 11c. Band-Pass Filter Decimate by 32

Figure 12a shows the frequency response of the digital filter in both low-pass and band-pass modes. Due to the sampling nature of the convertor, the pass band response is repeated about the input sampling frequency, Fsample and at integer multiples of Fsample. Out of band noise or signals coincident with any of the filter images are aliased down to the pass-band. However, due to the AD7723's high oversampling ratio, these bands occupy only a small fraction of the spectrum, and most broad-band noise is attenuated by at least 90 dB. In addition, as shown in Figure 12b, with even a low order filter, there is significant attenuation at the first image frequency. This contrasts with a normal Nyquist rate converter where a very high order anti-alias filter is required to allow most of the band width to be used while ensuring sufficient attenuation at multiples of Fsample.

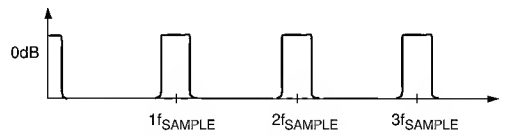


Figure 12a. Digital Filter Frequency Response

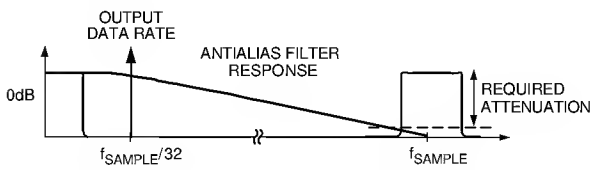


Figure 12b. Frequency Response of Antialias Filter

APPLYING THE AD7723

Analog Input Range

The AD7723 has differential inputs to provide common mode noise rejection. In unipolar mode the analog input range is 0 to 8/5 * VREF2 while in bipolar mode the analog input range is +/- 4/5* V_{REF2}. The output code is 2s compliment binary in both modes with 1 LSB = 61 uV. The ideal input/output transfer characteristics for the two modes are shown in Figure 13 below. In both modes the absolute voltage on each input must remain within the supply range AV_{SS} to AV_{DD}. The bipolar mode allows either single-ended or complimentary input signals.

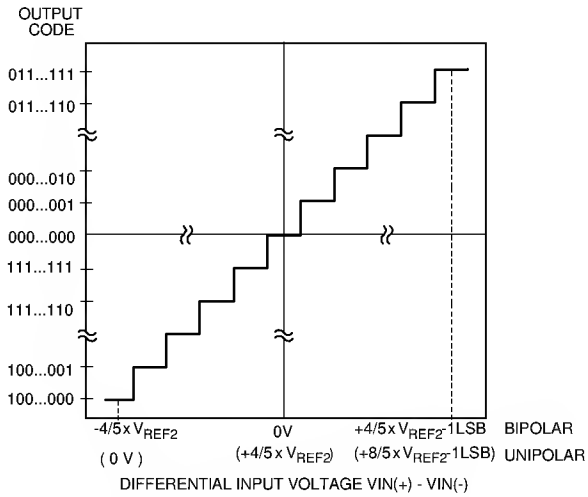


Figure 13. Bipolar (Unipolar) Mode Transfer Function

Analog Input

The analog input of the AD7723 uses a 'switched capacitor' technique to sample the input signal. For the purposes of driving the AD7723, an equivalent circuit of the analog inputs is shown in Figure 14. Each half clock cycle, two highly linear sampling capacitors are switched to both inputs, converting the input signal into an equivalent sampled charge. A signal source driving the analog inputs must be able to source this charge, while also settling to the required accuracy by the end of each half clock phase.

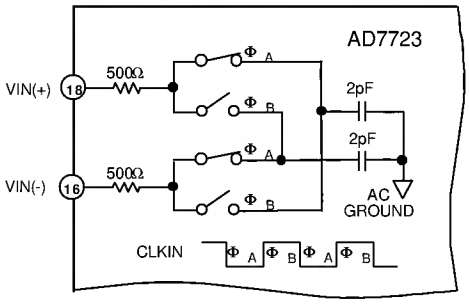


Figure 14. Analog Input Equivalent Circuit

Choice of op amp will be critical to achieving the full performance of the AD7723. The op amp must not only have to recover from the transient loads that the ADC imposes on it but must also have good distortion characteristics and very low input voltage noise. Where a current feedback op amp is chosen, input current noise is also important. Although the high OSR of the ADC results in most of the op amp wide band noise being removed by the digital filter, the high bandwidth nature of the input sampling network can result in op-amp noise at several of the passband images being aliased down into the passband. (See figure 12a).

Placing an RC filter between the drive source and the ADC inputs, as shown in Figures 15a and 15b, has a number of beneficial affects. Transients on the op amp outputs are significantly reduced: Instantaneous charge required to charge the internal sampling caps is provided by the external capacitor rather than the op-amp output. The op amp now only has to supply a nominally constant current to 'top up' the external capacitor. Also input circuit noise at the sample images is now significantly attenuated, improving the SNR. The external resistor serves to isolate the external capacitor from the op amp output, making it a friendlier load to drive while also isolating the op amp output from any remaining glitches on the capacitor. The capacitors, C1 in Figure 15a source both common mode and differential charge out of the ADC inputs. Capacitor C2 in Figure 15b sources differential charge out of the ADC inputs while the much smaller caps, C1 absorb any common mode charge. Best results have been achieved with the circuit in Figure 15b. To avoid coupling noise from the ground plane into the analog inputs, connect the two capacitors shown in Figure 15 to exactly the same point on the ground plane. This RC network should be arranged in a symmetric pattern. The average value of this current in the resistor is given by Equation 1.

$$I_{IN} \approx \left[V_{IN}(+) - V_{IN}(-)\right] \times 2 \times f_{CLKIN} \times 2pF \qquad (1)$$

By experimenting with different filter values the optimum performance can be achieved for each application. As a guide line the RC time constant (R*C) should be less than 1/4 the clock period to avoid nonlinear currents from the ADC inputs being stored on the external capacitor and degrading distortion. This restriction means that this filter can not form the main anti-alias filter for the ADC.

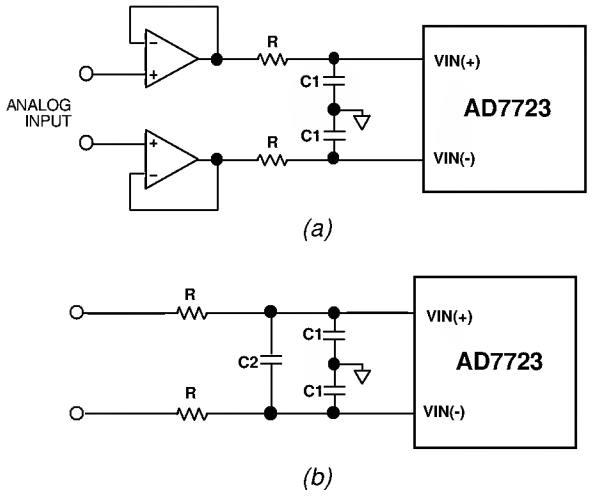


Figure 15. Input RC Networks

Driving the Analog Inputs

To interface the signal source to the AD7723 analog inputs, some signal conditioning is generally required. The very high input bandwidth and high resolution of the AD7723 means that considerable care has to be taken to avoid degrading the integrity of the signal chain. Even the thermal noise of the resistors has to be considered. Since the analog input is sampled as a differential voltage, common-mode noise at the analog input is rejected by the very high common-mode rejection of the AD7723.

Figures 16 and 17 show examples of two circuits with the AD7723 operating in bipolar mode using its internal reference. The RC network between the op amp outputs and input to the AD7723 are required to improve distortion and SNR as described in the Analog Input section.

The circuit shown in Figure 16 is well suited for systems in which the bipolar input is referenced to analog ground and requires proper level-shifting. The analog input, AIN, creates a 0.5 V to 4.5 V signal at the VIN(+) pin to form a +/-2 V differential signal around the initial 2.5 V bias of VIN(-).

Figure 17 shows a cross-coupled differential driver circuit best suited for systems where there is no information in the signal at dc. In the circuit shown, a 2 V_{P-P} analog signal source is ac coupled to produce a 4 V_{P-P} differential signal across the differential input of the AD7723. The internal 2.5 V reference of the AD7723 is used to set common-mode voltage of the differential circuit. The closed loop gain of the circuit can be easily set by R_{IN} and R_F. Vin(+) and VIN(-) are simultaneously driven with two equal signals that are in and out of phase versions of the input signal, AIN. The symmetrical nature of the circuit has the advantage of creating an input signal for the ADC that minimizes the even order distortion products of the amplifiers. Since the signal swing at the output of each op amp is only 2 V_{P-P}, (1.5 V to 3.5 V) the AD8047 can be used with a single +5 V power supply without headroom limitations. For more insight into the operation of this cross-coupled driver, please refer to the AD8002 and AD8042 datasheets.

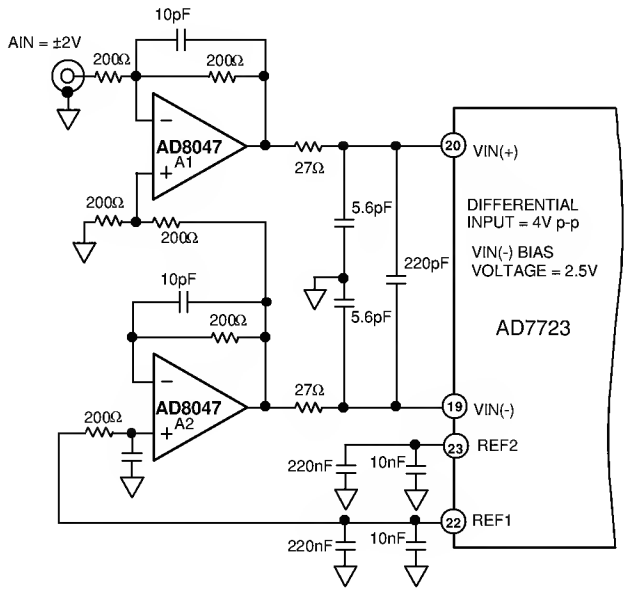


Figure 16. Single-Ended Input Circuit for Bipolar Operation

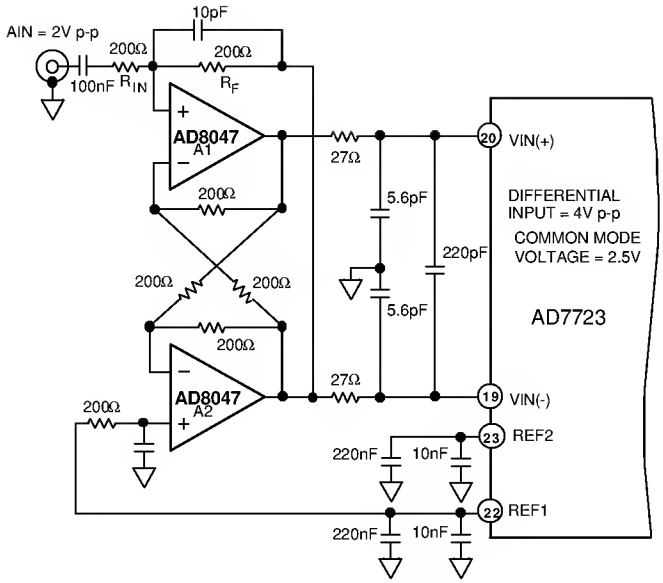


Figure 17. Single-Ended to Differential Input Circuit for Bipolar Mode Operation

Applying the Reference

The reference circuitry used in the AD7723 includes an on-chip 2.5 V band gap reference and a reference buffer circuit. The block diagram of the reference circuit is shown in Figure 18 The internal reference voltage is connected to REF1 through a 3 kΩ resistor and is internally buffered to drive the analog modulator's switched cap DAC (REF2). When using the internal reference a 220nF and 10 nF capacitor is required between REF1 and AGND to decouple the bandgap noise. If the internal reference is required to bias external circuits, use an external precision op amp to buffer REF1.

Where gain error or gain error drift require the use of an external reference, the reference buffer in Figure 18 can be turned off by grounding the REF1 pin and the external reference can be applied directly to pin REF2. The AD7723 will accept an external reference voltage between 1.2V to 3.15V. By applying a 3V rather than a 2.5V reference, SNR is typically improved by

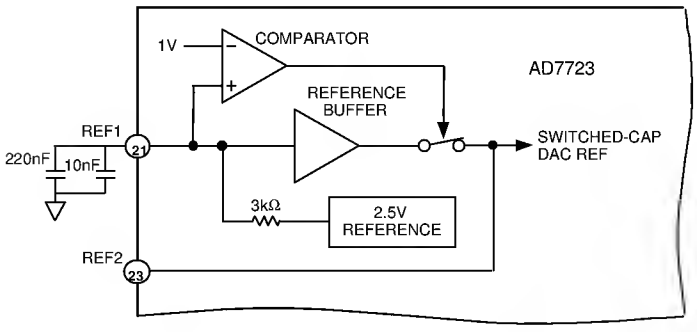


Figure 18. Reference Circuit Block Diagram

about 1 dB. Where the output common mode range of the amplifier driving the inputs is restricted, the full scale input signal span can be reduced by applying a lower than 2.5V reference. For example, a 1.25V reference would make the bipolar input span+/- 1V, but would degrade SNR.

In all cases, since the REF2 voltage connects to the analog modulator, a 220nF and 10 nF capacitor must connect directly from REF2 to AGND. The external capacitor provides the charge required for the dynamic load presented at the REF2 pin (Figure19.)

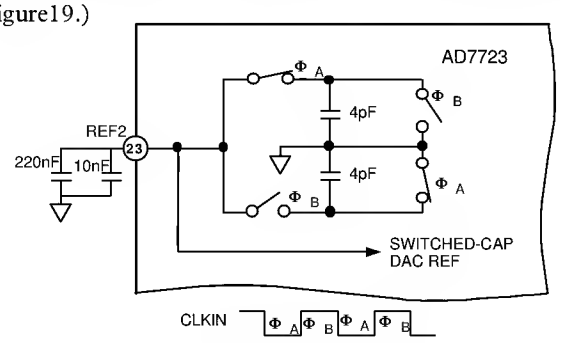


Figure 19. REF2 Equivalent Input Circuit

The AD780 is ideal to use as an external reference with the AD7723. Figure20 shows a suggested connection diagram. Grounding pin 8 on the AD780 selects the 3 V ouput mode.

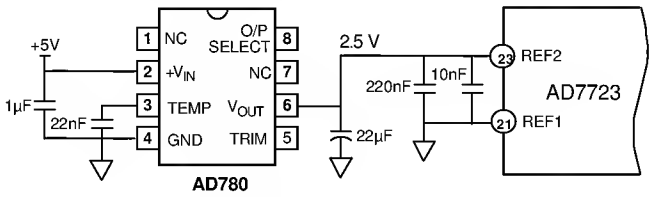


Figure 20. External Reference Circuit Connection

SERIAL INTERFACE

The AD7723's serial data interface can operate in three modes depending on the application requirements. The timing diagrams in Figures 3, 4, and 5 show how the AD7723 may be used to transmit its conversion results. Table I. shows the control inputs required to select each serial mode, the allowable conversion rates, and the digital filter operating mode. The AD7723 operates solely in the master mode providing three serial data output pins for transfer of the conversion results. The serial data clock output, SCO, serial data output , SDO, and frame sync output, FSO, are all synchronous with CLKIN. FSO is continuously output at the conversion rate of the ADC.

Serial data shifts out of the SDO pin synchronous with SCO. The FSO is used to frame the output data transmission to an external device. An output data transmission is either 16 or 32 SCO cycles in duration (refer to Table I.). The serial data shifts out of the SDO pin MSB first, LSB last, for a duration of 16 SCO cycles. In Serial Mode 1 the next 16 SCO cycles SDO outputs zeros.

In Serial Mode 1, the control input, SFMT, can be used to select the format for the serial data transmission. FSO is either a pulse, approximately one SCO cycle in duration, or a square wave with a period of 32 SCO cycles, depending on the state of the SFMT(Refer to figure 3). The clock format pin, CFMT, simply switches the phase of SCO .

With a logic low level on SFMT and CFMT set low (Figure 3), FSO pulses high for one SCO cycle at the beginning of a data transmission frame. When FSO goes low the MSB is available on the SDO pin after the rising edge of SCO and the serial data can be latched on the SCO falling edge.

With a logic high level on SFMT and CFMT set low (Figure 3), the data on the SDO pin is available after the rising edge of SCO and can be latched on the SCO falling edge. FSO goes low at the beginning of a data transmission frame when the MSB is available and returns high after 16 SCO cycles.

The Frame Sync Input, FSI can be used if the AD7723 conversion process must be synchronized to an external source. FSI is an optional signal; if FSI is grounded or tied high frame syncs are internally generated. Frame sync allows the conversion data presented to the serial interface to be a filtered and decimated result derived from a known point in time. FSI can be applied once after power-up, or it can be a periodic signal, synchronous to CLKIN at an exact integer multiple of the output word rate, occurring every 32 CLKIN cycles. When FSI is applied for the first time, or if a low to high transition is detected that is not synchronized to the output word rate, the next 32 conversion should be considered invalid while the digital filter accumulates new samples. A common frame sync signal can be applied to two or more AD7723s to synchronize them to a common master clock.

Two Channel Multiplexed Operation

Three additional serial interface control pins, DOE, TSI, and CFMT are provided. The connection diagram in Figure 21 shows how they are used to allow the serial data outputs of two AD7723s, operating in Serial Mode 1, to easily share one serial data line and have synchronously sampled inputs. Since a serial data transmission frame lasts 32 SCO cycles they can share a single data line by alternating transmission of their 16-bit output data onto one SDO pin.

The Data Output Enable pin, DOE, controls SDO's output buffer. When the logic level on DOE matches the state of the TSI pin, the SDO output buffer drives the serial data line, otherwise the output of the buffer goes high-impedance. The serial format pin, SFMT, is set high to chose the frame sync output format. The clock format pin, CFMT, is set low so that serial data is made available on SDO after the rising edge of SCO and can be latched on the SCO falling edge.

The Master device is selected by setting TSI to a logic low and connecting its FSO to DOE. The Slave device is selected with its TSI pin tied high and both its FSI and DOE controlled from the Master's FSO. Since the FSO of the Master controls the DOE input of both the Master and Slave, one ADCs SDO is active while the other is high-impedance (Figure 22). When the Master transmits its conversion result during the first 16 SCO cycles of a data transmission frame, the low level on DOE sets the slave's SDO high-impedance. Once the Master completes transmitting its conversion data, its FSO goes high, triggers the Slave's FSI to begin its data transmission frame.

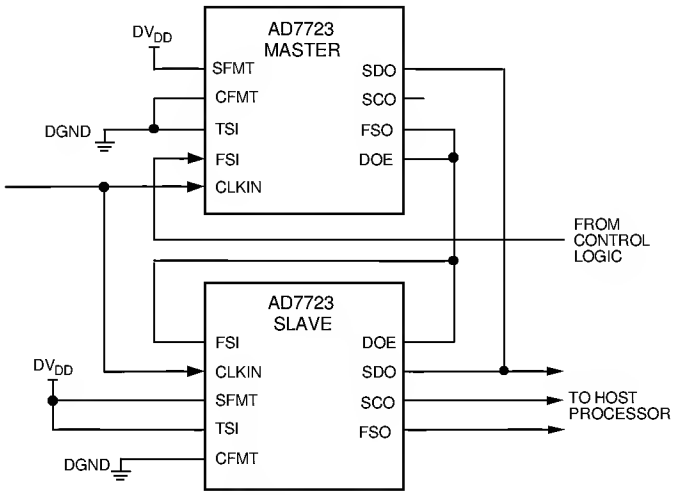


Figure 21. Serial Mode 2 Connection for Two Channel Multiplexed Operation

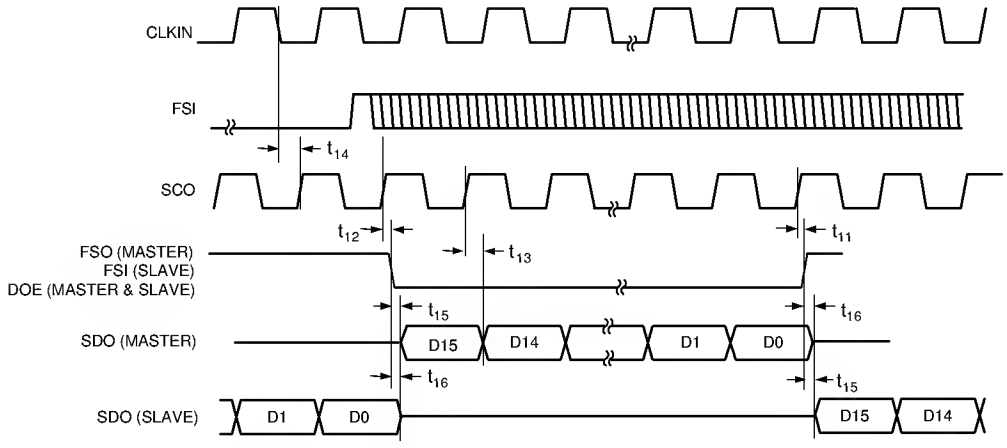


Figure 22. Serial Mode 1 Timing for Two Channel Multiplexed Operation

Grounding and Layout

The analog and digital power supplies to the AD7723 are independent and separately pinned out to minimize coupling between analog and digital sections within the device. All the AD7723 AGND and DGND pins should be soldered directly to a ground plane to minimize series inductance. In addition, the AC path from any supply pin or reference pin (REF1 and REF2) through its decoupling capacitors to its associated ground must be made as short as possible(Figure23). To achieve the best decoupling, place surface mount capacitors as close as possible to the device, ideally right up against the device pins.

All ground planes must not overlap to avoid capacitive coupling. The AD7723's digital and analog ground planes must be connected at one place close to the device. Any external logic connected to the AD7723 should use a ground plane separate from the AD7723's digital ground plane. These two digital ground planes should also be connected just at one place.

Separate power supplies for AVDD and DVDD are also highly desirable. The digital supply pin DVDD should be powered from a separate analog supply, but if necessary DVDD may share its power connection to AVDD. Refer to the connection diagram (Figure 23). The 10 ohm resistors in series with both the AV_{DD1} and DV_{DD} pins are required to reduce ringing on the power supplies caused by fast switching logic. The ferrites are also recommended to filter high frequency signals from corrupting the analog power supply.

A minimum etch technique is generally best for ground planes as it gives the best shielding. Noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. In waveform sampling and reconstruction systems the sampling clock (CLKIN) is as vulnerable to noise as any analog signal. CLKIN should be isolated from the analog and digital systems. Fast switching signals like clocks should be shielded with their associated ground to avoid radiating noise to other sections of the board, and clock signals should never be routed near the analog inputs.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7723 to shield it from noise coupling. The power supply lines to the AD7723 should use as large a trace as possible (preferably a plane) to provide a low impedance path, and reduce the effects of glitches on the power supply line. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board.

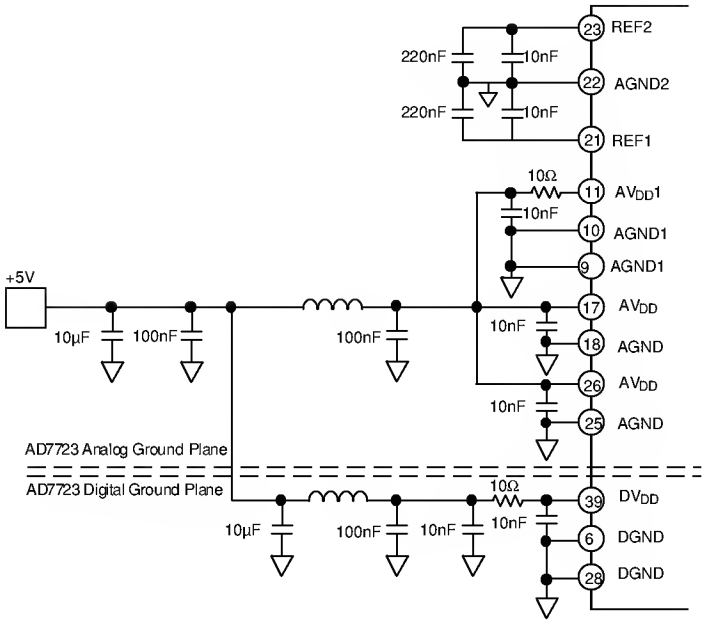


Figure 23. Reference and Power Supply Decoupling